INIVEN

**INSTRUCTION MANUAL**

# Model IAR ANALOG RECEIVER

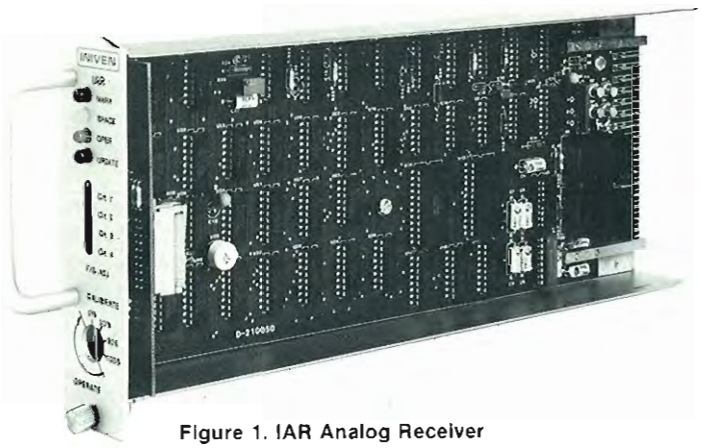


Figure 1. IAR Analog Receiver

## 1. DESCRIPTION. (See Figure 1)

1.1 The INIVEN™ IAR Analog Receiver used in conjunction with an INIVEN™ IAT Analog Transmitter comprise a 4-channel, high performance, solid-state, analog digital/digital-analog subsystem. The IAT and IAR provide from 1 to 4 analog variables plus 4 status or alarm conditions to be transmitted over a single INIVEN™ Series 30 FSK Tone Channel.

1.2 The IAR receives a 24-bit data-word, consisting of 12 bits of digitized analog values, 2 bits of channel address, 4 bits of status, and 6 bits of BCH (Bose-Chaudhuri-Hocquenghem) error detection code, followed by a single sync interval. The IAR accepts tone signals via a high-noise-immunity Schmitt-trigger input. Then the IAR performs validity checks and outputs the information. Analog outputs are PNP, high-gain, open-collector. Darlington pairs are used to activate meters and controls. Status outputs are open-collectors.

## 2. SPECIFICATIONS

**Analog Outputs:** 1, 2, 3, or 4

**Analog Resolution:** 12 bits (0.024%/step).

**Analog Accuracy:** ±.1% @ 25°C
.5% @ -30°C to +60°C

**Analog Linearity:** ±.05% @ 25°C
.1% @ -30°C to +60°C

**Output Range:** 0-1, 0-5, 1-5, 0-20, 4-20, 0-50, 10-50 mA standard ranges. Any nonstandard up to 50 mA selected by internal resistor. External supply to 40V may be used to drive outputs.

**Status Outputs:** Open collector to B+, 600 mA maximum, 4 status outputs, or 3 status, one data-fail output.

**Input Keying:** Optimized for INIVEN™ IR-30 FSK Receiver outputs with IA-11 Adapters.

**Data-Fail Criterion:** Selectable elapsed time period of 5 to 40 seconds between failure to receive valid data and actuation of data-fail circuit.

**Operating Temperature:** -30°C to +60°C (-22°F to +140°F)

**Power Requirements:** 12 Vdc @ 300 mA (Does not include analog or status drive current.)

**Operating Humidity;** 0-90% non-condensing

**Dimensions:** See Figure 5

**Weight:** 1.75 lb. approximately (.79 kg)

## 3. FEATURES

3.1 **Output Level Calibration.** Output level calibration adjustments accessible on the front panel of the IAR allow calibration of outputs to 0%, 20%, 80% and 100% of full-scale.

3.2 **Indicators.** Mark, Space, Data Update and Operate LED indicators are mounted on the front panel.

3.3. **Data-Fail.** Outputs stay at last valid value or reset to zero, strap selectable.

## 4. THEORY OF OPERATION. (See Figures 2 and 3)

4.1 The IAR consists of a data input circuit, clock, BCH code generator, data check circuit, memory load circuit, RAM memory, pulse width modulator, voltage reference, analog output circuit, status output circuit, and reset circuit.

4.2 **Data Input Circuit.** The data input circuit consists of inverters U1, counter U41, shift registers U10, U8, and U12, XOR gate U26D, flip-flop U29A, multivibrator U25A, OR gates U18C and U18D, AND gates U30C and U30D, and associated circuitry.

4.3 The Mark and Space data from the IR-30 Tone Receiver are applied to Schmitt-trigger inverters U1D and U1E through limiting resistors to eliminate bias and harmonic distortion. These inverted Mark and Space data are inverted again by U1C and U1F and used to drive the Mark and Space LEDs on the front panel through U1A and U1B. The outputs from U1C and U1E are applied to OR gate U18C resulting in a data stream which

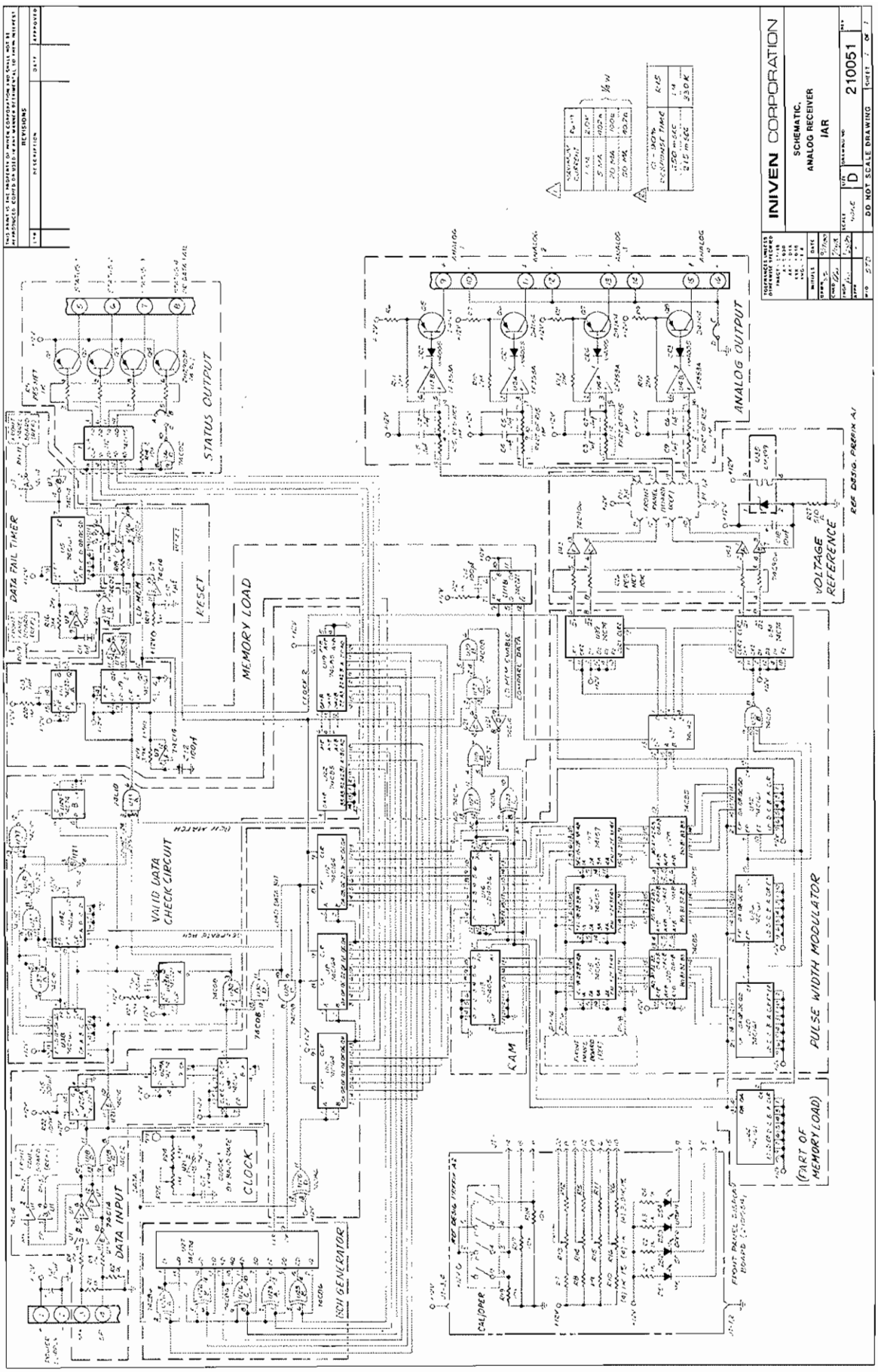



Figure 2. IAR Analog Receiver—Schematic Diagram

is routed to the BCH generator and U26D whose inverted output goes to the shift register composed of U8, U10, and U12. The Mark and Space data from U1C and U1F are also applied to OR gate U18D, resulting in a HIGH output when either Mark or Space is present. The signal from U18D is applied to AND gate U30D and U21E whose inverted output goes to U30A in the valid data check circuit. This signal enables U30D when data is present, and U30A during a sync interval. The signal from U21E is routed to the valid data check circuit. The signal from U18D also triggers multivibrator U25A to generate a pulse to clear flip-flop U25A whose output causes U41 to load at the next clock pulse. U41 is preset to a count of 12 and proceeds to count when a load is applied. When the count reaches 15, the carry output goes HIGH at pin 15, and this pulse is gated through U30A or 30D, depending on whether data or a sync period is detected. The data pulses from U30D are used to clock the shift register. When the GENERATE BCH signal is received from the valid data check circuit, the data pulses are routed through U30C to clock the BCH generator.

4.4 **Clock Circuit.** The clock circuit is composed of inverter U21B, resistor R24, potentiometer R25, and capacitor C17. It is adjusted to a frequency eight times (8X) the desired baud rate.

4.5 **BCH Generator.** The BCH code generator consists of flip-flops U27 and XOR gates U23A, U23B and U26A through U26C.

4.6 The data stream from U18C in the data input circuit is applied to U26A. The clock pulse (count=18) from U30C in the data input circuit is applied to U27-9. The generator is cleared by a pulse U27-1 from U25B in the valid data check circuit during the sync period. The BCH generator produces a code that matches the BCH code received from the transmitter and is routed to the valid data check circuit.

4.7 **Valid Data Check.** The data check circuit consists of NAND gate U37, counters U38, and U42, comparators U22 and U19, AND gate U30A, OR gate U18A, inverter U21B, multivibrator U25B, and flip-flop U29B.

4.8 The Mark or Space pulses from U21E in the data input circuit are applied to the clock input of the counter U38 and U42 to be counted. When a count of 24 pulses is detected by NAND gate U37B and OR gate U18A, a LOW output from U18A is routed to U21 whose inverted output HIGH goes to NAND gate U33-3. If any other count than 24 pulses is received before the sync pulse by the gates, U37A will disable the counters and U33-3 goes LOW. Also at the count of 18 pulses, the counter outputs go to U37C which clears flip-flop U29B. The output (GENERATE BCH) is routed to U30C in the data input circuit to disable the clock pulse to the BCH generator. A sync signal output from U30A is applied to U33-4 (sync) and also triggers multivibrator U25B to generate a pulse at pin 12 to clear the counters. U25B output pulse is routed to clear BCH generator and also sets U29 whose output enables the BCH generator.

4.9 Compartor U19 and U22 compare the BCH code from BCH generator with the last six bits in the shift register, U10, in data input circuit. When these bits match, U22-3 output goes HIGH to U33-5 (BCH MATCH). When the three criteria (count=25, sync detection, and BCH code match) are met, U33A enables the memory load circuit to accept data.

4.10 **Memory Load and RAM Circuits.** The memory load circuit consists of counters U9 and U44, multivibrator U11, and parts of U7, U30, U23, U18, and U21.

4.11 The pulsed output (LOW) from NAND gate U33A in the valid data check circuit is applied to U11, which generates a longer pulse to drive the update LED on the front panel and to U16B in the

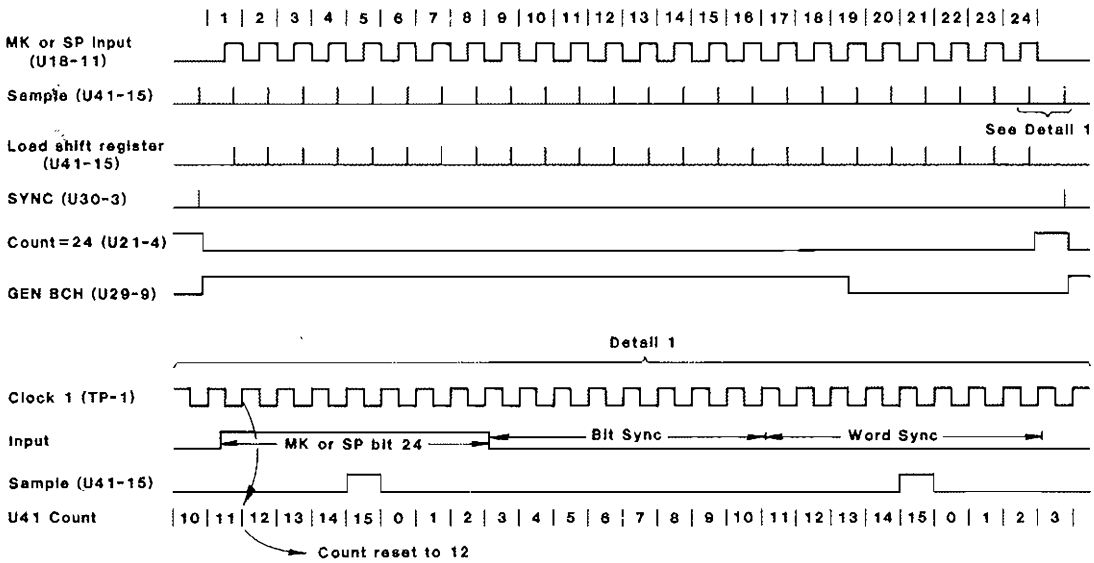



Figure 3. IAR Analog Receiver—Timing Diagram

data fail timer circuit. The output of U33A also clears U9 to set up the memory load circuit to load the data into the proper location.

4.12 Inverter U7F, resistor R19 and capacitor C12 form an oscillator circuit whose output is approximately a 1MHz signal (CLOCK 2) which is routed to clock counter U9. After U9 is cleared by a pulse from U33A, the counter counts to 8, then QD(U9-11) goes HIGH and is routed to inverter U7C whose output is LOW to U9-10, this will disable the counter. Output QC(U9-12) produces a pulse (LD MEM) that lasts exactly four periods of CLOCK 2. This pulse is routed to U33C and to flip-flop U2 in the status output circuit.

4.13 The RAM circuit consists of 4X8-bit static CMOS Random-Access Memories U13 and U14.

4.14 Counter U44, clocked by CLOCK 2, output signals $A0^1$ and $A1^1$ are applied to the decoder U31 with $A1^1$ as a clock for the counter in the pulse width modulator circuit. $A0^1$ and $A1^1$ are also used to address the four locations in the RAM. In the four clock periods of the LD MEM pulse, the RAM is addressed at each location. When RAM address $A0^1$ and $A1^1$ match received channel address bits A0 and A1, XOR gates U23C and U23D go LOW, which causes OR gate U18B to go LOW and is then routed to the inverter U21C. Meanwhile multivibrator U11B, triggered by CLOCK 2, produces a 200 nanosecond pulse (LD MEM ENABLE) to ensure that the RAM access time is not violated. When three inputs (a two-clock cycle LD MEM pulse, a one-cycle address match and a 200-nsec LD MEM ENABLE pulse) are matched in high polarity at the NAND gate U33C the output is routed to AND gate U30B whose power reset input is HIGH causing the output to go LOW which is applied to inverter U21D. This output signal is a 20-nsec HIGH pulse applied to the RAM write input chips U13 and U14 to load new data into the selected address. The compare data pulse (U11B-12) is routed to the decoder chip (U31) in the pulse width modulator circuit.

4.15 **Reset Circuit.** The reset circuit consists of inverter U7E, NOR gate U6A and associated components. At power up, Schmitt-trigger inverter U7E is held HIGH by a RC time-constant for a time period which goes to U6B in the data fail timer circuit and to U6A, whose output is the RESET signal. RESET is routed to clear U2 in the status output circuit and to the shift register U8 and U12 in the data input circuit. At the same time, it forces U30B to go LOW which goes to inverter U21D in the valid data check circuit, whose output is a HIGH pulse to the RAM write inputs. Therefore the RAM is loaded with zeros from the shift register outputs in the data circuit. This zeros output will ensure that both the status and analog outputs start at zero.

4.16 If jumper F-G is installed, the data fail timer activates the reset circuit to clear the outputs when a data-fail condition occurs.

4.17 **Data Fail Timer.** The data fail timer consists of counter U5; inverters U7A, U7B and U7D; and NOR gates U6A and U6B. Inverter U7D, capacitor C11 and resistor R16 form a 0.2Hz oscillator circuit whose output is used to clock counter U5. The counter is cleared to zero at power-up by inverter U7E output in the reset circuit or by the transfer pulse from U11A output in the memory load circuit via NOR gate U6B. If a clearing pulse is not received, U5 counts until the select output (QB, QC, or QD; by jumper) goes HIGH which is routed to inverter U7B. The output goes to U5-7, which will disable the counter, and to U7A whose output turns the OPER LED on the front panel off. The U5 select output is also applied to U6C in the status output circuit. If jumper F-G is installed, the outputs of U5 are cleared by activation of either the reset circuit or the memory load circuit.

4.17A The status output consists of flip-flop U2, transistors Q1 through Q4, NOR gate U6C and the resistor network. The status data from the shift register in the data input circuit is applied to U2 whose output is clocked out by the clock pulse (LD MEM) from U9 in the memory load circuit. The output signal is routed to the base of the transistor with an open-collector to external connection. If jumper A-B is removed and B-C is installed, the data fail is routed to U6C whose output goes to the fourth status point. This output is energized on data fail.

4.18 **Pulse Width Modulator.** The pulse width modulator consists of multiplexers U15, U16, and U17; 4-bit comparators U20, U24, and U28; counters U32, U36, and U40; BCD decoder U31; dual flip-flops U34 and U39; and NAND gate U33B.

4.19 Multiplexers U15, U16 and U17 form a 12-bit one-of-two multiplexer. When the front panel CAL/OPER switch is in one of the switching positions 4 through 9, the select inputs are HIGH: therefore the data from the RAMs circuit is transferred to the multiplexer output. When the CAL/OPER switch is in one of the switching positions 0 through 3, the select inputs are LOW. The switch position determines what digital word is transferred (corresponding to 0%, 20%, 80% or 100% of full scale reading) to allow meter calibration from the front panel for each individual channel. Counter U32, U36 and U40 form a 12-bit counter clocked by the $A1^1$ signal from U44-13 in the memory load circuit. The 12-bit counter counts from 0 to 4095 approximately 60 times each second which advances one count for every four counts of the CLOCK 2. Comparators U20, U24 and U28 compare the data from the multiplexers to each count of the counter output for each analog address. If the counter output is less than the data, U28-13 output remains HIGH, but when counter output is greater or equal to the data, this output goes LOW which goes to the decoder. Decoder U31 selects the proper output using address lines $A0^1$ and $A1^1$ only when U28 outputs and COMPARE DATA from U11B in memory load

circuit are LOW. When the data pertaining to a given channel is equal to or less than the counter output, a negative pulse appears at the appropriate output of decoder U31. This LOW pulse clears the selected flip-flop of U34 and U39. At the end of the count of 4095 by the counter, it outputs to NAND gate U33B whose output (a negative pulse) is applied to reset the flip-flop to a HIGH output. Since the inverted outputs of U34 and U39 are used, the result is a series of pulses which begin LOW and go HIGH for each channel when data and count are matched. The LOW duty cycle corresponds to the data percent of the full scale. The pulse frequency is approximately 60 Hz.

4.20 **Voltage Reference Circuit.** The voltage reference circuit consists of precision voltage reference U35, buffer U43, resistors R26 and R27, capacitor C18, and the scaling resistors and potentiometers located on the front panel board PCB A2.

4.21 A temperature-controlled 6.95v reference Vref), U35, is used as a negative power supply for open-drain buffers U43. R26 interfaces the 0 to 12 volt pulses from either U34 or U39 in the pulse width modulator circuit with U43 whose output pulse swing is approximately 5 to 12 volts. The outputs of U43 swing from +12v to +12v minus Vref, and thus are stable even if the +12v supply changes. The signals are applied to the variable scaling resistors located on the front panelboard to provide calibration of the full scale output. The scaled pulses are then routed to the filter in the analog output circuit.

4.22 **Analog Output Circuit.** The analog output circuit consists of low-pass filter components R15 and C2 through C9, operational amplifiers U3 and U4, transistors Q5 through Q8, current scaling resistors R6 through R9, and diodes CR1 through CR4.

4.23 Scaled pulses from the voltage reference circuit are filtered to produce a dc level that varies from +12 volts for zero output to 10 volts for full-scale output. The amplifiers and output transistors are connected to give 0 to 2 volts across the current-scaling resistors. Darlington transistors ensure that virtually all the current flowing through these resistors is delivered to the outputs. CR1 through CR4 provide an extra voltage drop which guarantees the amplifiers are able to turn the output transistors completely off under all conditions.

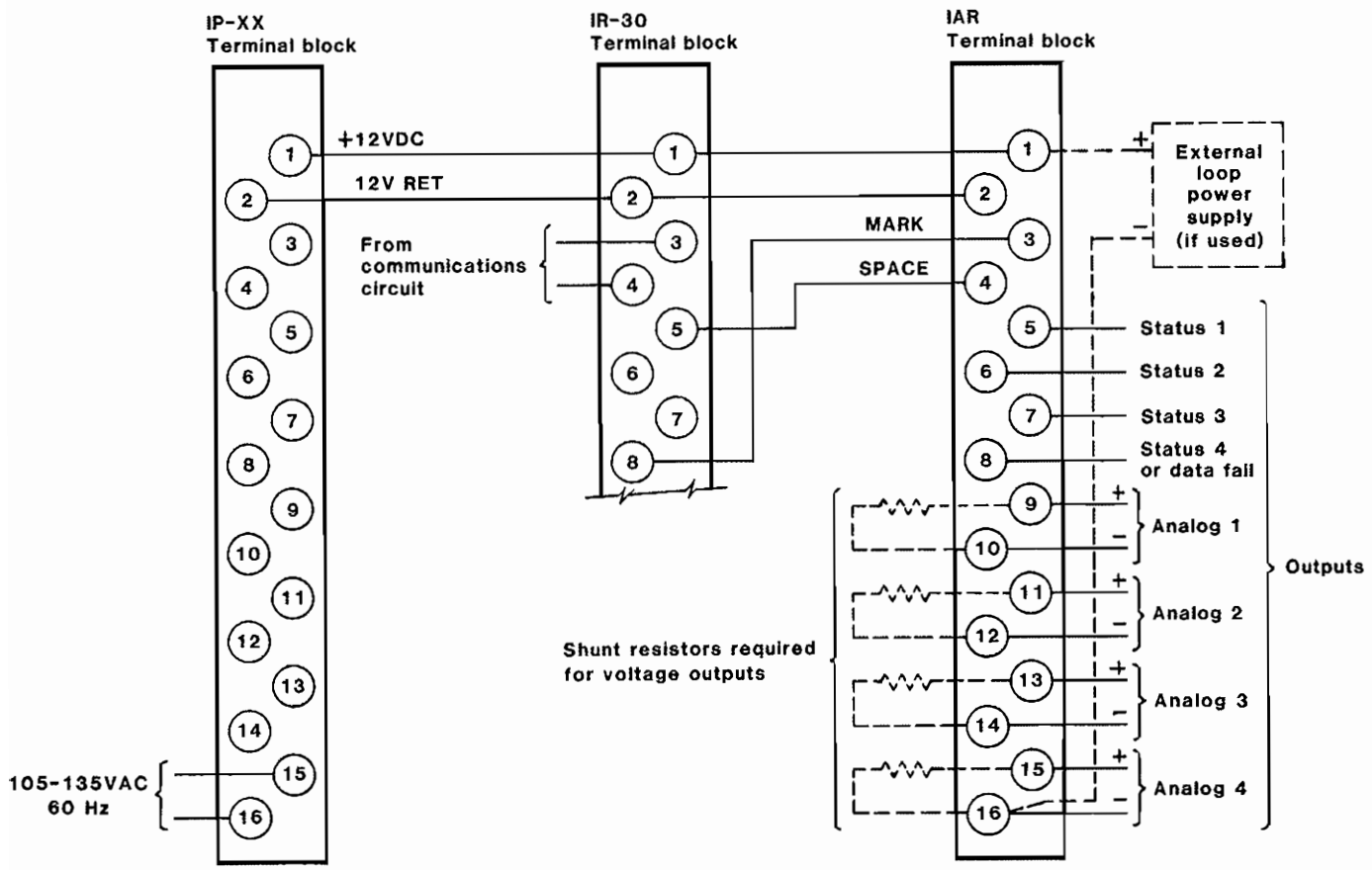



Figure 4. Electrical Installation

## 5. INSTALLATION

5.1 **Unpacking.** Unpacking and handling of the IAR Analog Receiver should be consistent with procedures used in handling electronic equipment.

5.2 **Inspection.** Visually inspect the analog receiver for damage from rough handling and faulty packing. Visually inspect for:

(1) Loose wires
(2) Deformation in the frame
(3) Faceplate damage
(4) Evidence of moisture or condensation within the units.
(5) Loose hardware or parts which evidence improper handling.

5.3 **Mechanical Installation.** The IAR is shipped with the terminal block plugged into the rear of each unit with four 6-32 screws partially installed. The IAR Analog Receiver is normally mounted in standard INIVEN™ Tone Frames.

5.4 Install the IAR as follows:

(1) Leave terminal block plugged in, as shipped, on rear of unit.
(2) Remove four 6-32 screws from terminal block.
(3) While inserting IAR into tone frame align captive screw at bottom of face-plate with mounting hole in frame.
(4) Secure IAR to frame using captive screw on face-plate.
(5) At rear of frame, use 6-32 screws removed in step (2) to secure terminal block to tone frame.

The IAR can now be removed and re-installed in frame using the front panel captive screw.

5.5 **Electrical Installation.** All electrical connections are made to the terminal block at the rear of the frame (see Figure 4 and Table 5-1).

5.6 **12-Volt Power Supply.** If a separate 12-volt power supply is used in place of the IP-XX, negative of the 12-volt supply must be common to terminal 2 of the IAR as shown in Figure 4.

**Table 5-1 Terminal Block Connections**

| TERMINAL | FUNCTION |
|---|---|
| 1 | Positive (+) side of 12 Vdc power supply input. |
| 2 | Negative (-) side of 12 Vdc power supply input. |
| 3 and 4 | Mark and Space Input |
| 5 through 8 | Status Outputs 1 through 4. |
| 9 through 16 | Analog Outputs 1 through 4. |

5.7 **External Loop Power Supply.** Using the IP-XX power supply the IAR operates with 10 volts of compliance. If more compliance is required, an external loop power supply of up to 40 volts maximum may be used. If an external loop power supply is used, cut the etch between D and E on printed circuit board A1 (see Figure 6). Connect the positive output of the external loop power supply to terminal 1 and the negative to terminal 16 as shown in Figure 4. Loop compliance is 2 volts less than the power supply voltage.

5.8 **Voltage Output.** If a voltage output is required, external shunt resistors must be used to convert the current outputs.

5.9 **Electrical Grounding.** It is recommended that the chassis of each tone unit be grounded to reduce ground loop interference effects. When the tone unit is housed in a standard INIVEN™ Tone frame, a good earth-ground to the rack or other equipment, in which the frame is installed, is sufficient. When the individual tone units are operated out of the frame, each tone unit chassis should be connected to earth-ground.

5.10 Station batteries or other power supplies can be employed in place of standard INIVEN™ Power Supplies.

5.11 Clock Adjustment

The following equipment is required to set the clock rate of the IAR Analog Receiver.

| | | |
|---|---|---|
| **Extender Module** | **INIVEN** | **Model IE-5** |
| **Frequency Counter** | **Fluke** | **Model 1900A (or equiv.)** |

5.12 **Adjustment Procedure.** Adjust the IAR clock rate as follows:

(1) Loosen captive retaining screw and remove IAR from frame.
(2) Plug IAR into Extender Module.
(3) Install Extender Module in space vacated by IAR.
(4) Ground Frequency Counter to terminal 2 of connector of printed circuit board A1 (see Figure 6) and connect test probe to TP1.
(5) Frequency Counter should indicate a frequency eight times (8x) the baud rate, if not proceed to step (6). (8x 50 baud rate = 8 x 50 = 400 Hz)
(6) Rotate adjustment screw on potentiometer R25 to obtain the desired indication on Frequency Counter.
(7) Disconnect Frequency Counter from IAR.
(8) Unplug IAR from Extender Module and remove Extender Module from frame.
(9) Install IAR in frame and secure with captive screw.

5.13 **Output Calibration.** The analog outputs are calibrated via front panel F/S ADJ potentiometers and the CALIBRATE/OPERATE switch. Each channel may be calibrated to the desired full-scale level, similarly to the typical procedure for channel 1, as follows:

(1) Set CALIBRATE/OPERATE switch to 100%.
(2) Adjust the CH1 potentiometer to obtain a full-scale reading on the externally connected indicator (meter).
(3) Set CALIBRATE/OPERATE switch to percentage of full-scale which reflects minimum reading. (i.e. 4-20mA meter would reflect 20% as minimum reading).

(4) If external meter has a zero-adjustment, make the zero (low-end) adjustment.

(5) Set CALIBRATE/OPERATE to 100%. If full-scale indication has changed repeat steps (2) through (4) while making fine adjustments to CH1 potentiometer and meter.

5.14 **Data-Fail Modification.** From approximately 5 to 40 seconds may be allowed to elapse between failure to receive valid data and the OPER Indicator extinguishing. The standard configuration of the IAT permits a 35-40 second lapse after data-fail occurrence. To modify the elapsed time-period install jumpers on printed circuit board A1 (see Figure 6) in accordance with Table 5-2.

**NOTE**

**A Maximum of one jumper may be installed at any time.**

**Table 5-2**

| TIME PERIOD | JUMPER | CUT |
|---|---|---|
| 5-10 sec | K to L | H to L |
| 15-20 sec | J to L | H to L |
| 34-40 sec | H to L | |

5.15 **Data-Fail Reset Modification.** When a data-fail occurs, the outputs retain last valid data received. If it is desired to reset the outputs upon data-fail occurrence, install a jumper on printed circuit board A1 (see Figure 6) between F and G.

5.16 **External Data-Fail Indication Modification.** If it is desired to use an external circuit for data-fail indication, status 4 output is used. Proceed as follows:

(1) Cut the etch between A and B on printed circuit board A1 (see Figure 6).

(2) Install a jumper from B to C.

(3) Connect external indicator circuit to terminal 8 of terminal block. Terminal 8 will be energized upon data-fail occurrence.

5.17 **Data Update Rate Modification.** If very rapid update rates are required (more often than every 650 milliseconds), resistor pack R15 may be changed in accordance with the parts list of Figure 6. However; for update intervals less than 650 milliseconds, a similar modification should be made to the matching IAT Analog Transmitter for the system to perform satisfactorily.

5.18 **Output Current Range Modification.** The output current range of Analog 1 through Analog 4 is controlled by the value of resistors R6 through R9, respectively. Each output may be set to a desired range by changing the resistor in accordance with the parts list of Figure 6. For non-standard ranges the resistance value may be computed by R=2V/I, where I is the maximum current desired. The resistor should be type RN60C metal-film, 1%, 1/4 watt rating.

## 6. MAINTENANCE

6.1 The module you have purchased has been thoroughly inspected and tested in accordance with our specifications. The module does not require preventive maintenance.

6.2 Sections 6 of associated FSK receiver and transmitter instruction manuals contain maintenance and malfunction isolation check procedures for systems, receivers, and transmitters. Use those procedures as the first step in isolating troubles. When use of those procedures fail to locate the cause of the malfunction or the trouble is isolated to the IAR, refer to Section 4 of this instruction manual, for detailed theory of operation and the referenced schematics, as an aid in signal tracing.

| MAXIMUM CURRENT | R6 R9 | MAXIMUM EXTERNAL RESISTOR |
|---|---|---|
| 1MA | 2.0K | 9.0K |
| 5MA | 402Ω | 1.8K |
| 20MA | 100Ω | 450Ω |
| 50MA | 40.2Ω | 180Ω |

| 0 90% RESPONSE TIME | R15 |
|---|---|
| 650 MSEC | IM |
| 215 MSEC | 330K |

## 7. PARTS LIST

The following parts list is included to facilitate maintenance of the IAR Analog Receiver. All parts are listed in order of their reference designators as applicable. Figure 5 depicts the parts for the major components of the IAR. Figures 6 and 7 exhibit the parts for printed circuit board assemblies A1 and A2, respectively.

### 7.1 IAR ANALOG RECEIVER (See Figure 5)

| REF DESIG | DESCRIPTION | QTY | PART NUMBER | MFR |
|---|---|---|---|---|
| | PRINTED CIRCUIT BOARD ASSEMBLY A1 | | | |
| C1, C18 | •CAPACITOR, 10uf, 25V, 10% Tant | 2 | DT25V106K | |
| C2-C9 | •CAPACITOR, 0.1uf, 400V, 20%, Met. Poly | 8 | MPC33H104M | |
| C10, C13 | •CAPACITOR, 0.1uf, 50V, 20% Cer | 2 | 8121651-104M | |
| C11 | •CAPACITOR, 1uf, 50V, 20%, Cer | 1 | 8121651-105M | |
| C12, C14 | •CAPACITOR, 100pf, 100V, 20% Cer | 2 | 8121COG-101K | |
| C15, C16 | •CAPACITOR, .001uf, 100V, 20% Cer | 2 | KX7R102K200 | |
| C17 | •CAPACITOR, .0047uf, 200V, 20%, Met. Poly | 1 | MPL33F472M | |
| CR1-CR4 | •DIODE, 1A, 600V | 4 | 1N4005 | Motorola |
| P1 | •CONNECTOR, Plug, 20 Pin | 1 | CA-D20-SP100 | Circuit Assy |
| Q1, Q4 | •TRANSISTOR, PNP (TO-18) | 4 | 2N2907A | Motorola |
| Q5-Q8 | •TRANSISTOR, Darlington, PNP | 4 | D41K4 | General Electric |
| R1, R2, R21 | •RESISTOR, 1K, 1/4W, 5% | 3 | RCF07J102 | |
| R3, R4, R14, R18 | •RESISTOR, 10K, 1/4W, 5% | 4 | RCF07J103 | |
| R5 | •RESISTOR NETWORK, 1K, SIP, 8 Pin | 1 | 4308R102-103 | Bourns |
| R6-R9 | •RESISTOR, 1/4W, 1% | 4 | * | |
| R10-R13 | •RESISTOR, 2 Meg, 1/4W, 5% | 4 | RCF07J205 | |
| R15 | •RESISTOR NETWORK, DIP, 16 Pin | 1 | ** | |
| | •SOCKET, DIP, 16 Pin | 24 | 703-53160104 | |
| R16 | •RESISTOR, 3 Meg, 1/4W, 5% | 1 | RCF07J305 | |
| R17, R20 | •RESISTOR, 1 Meg, 1/4W, 5% | 2 | RCF07J105 | |
| R19 | •RESISTOR, 3.9K, 1/4W, 5% | 1 | RCF07J392 | |
| R22, R23 | •RESISTOR, 100K, 1/4W, 5% | 2 | RCF07J104 | |
| R24 | •RESISTOR, 33K, 1/4W, 5% | 1 | RCF07J333 | |
| R25 | •RESISTOR, Variable, 1 Meg, 20 Turn | 1 | 3299W-1-105 | Bourns |
| R26 | •RESISTOR NETWORK, 10K, SIP, 8 Pin | 1 | 4308R102-103 | |
| R27 | •RESISTOR, 510 ohm, 1/4W, 5% | 1 | RCF07J511 | |
| U1, U7, U21 | •INVERTER, Schmitt-Trigger, Hex | 3 | MM74C14N | Nat'l Semiconductor |
| U2 | •FLIP-FLOP, Quad | 1 | MM74C175N | Nat'l Semiconductor |
| U3, U4 | •AMPLIFIER, Operational, Dual | *** | LF353A | Nat'l Semiconductor |
| U5, U9, U32, U36 U38, U40-U42, U44 | •COUNTER, Binary | 9 | MM74C161N | Nat'l Semiconductor |
| U6 | •NOR GATE, 2-Input, Quad | 1 | MM74C02N | Nat'l Semiconductor |
| U8, U10, U12 | •SHIFT REGISTER, 8-bit | 3 | MM74C164N | Nat'l Semiconductor |
| U11, U25 | •MULTIVIBRATOR, Monostable, Dual | 2 | MM74C221N | Nat'l Semiconductor |
| U13, U14 | •RAM, CMOS, 4 x 8 static | 2 | CD4036AE | RCA |
| U15-U17 | •MULTIPLEXER, 2-input, Quad | 3 | MM74C157N | Nat'l Semiconductor |
| U18 | •OR GATE, Quad | 1 | MM74C32N | Nat'l Semiconductor |
| U19, U20, U22 U24, U28 | •COMPARATOR, Magnitude, 4-bit | 5 | MM74C85N | Nat'l Semiconductor |
| U23, U26 | •XOR GATE, 2-Input, Quad | 2 | MM74C86N | Nat'l Semiconductor |
| U27 | •FLIP-FLOP, Hex | 1 | MM74C174N | Nat'l Semiconductor |
| U29, U34, U39 | •FLIP-FLOP, Dual | *** | MM74C74N | Nat'l Semiconductor |
| U30 | •AND GATE, 2-Input, Quad | 1 | MM74C08N | Nat'l Semiconductor |
| U31 | •DECODER, BCD-to-Decimal | 1 | MM74C42N | Nat'l Semiconductor |
| U33, U37 | •NAND GATE, 3-Input, Quad | 2 | MM74C10N | Nat'l Semiconductor |
| U35 | •VOLTAGE REFERENCE, Precision | 1 | LM399HL | Nat'l Semiconductor |
| U43 | •BUFFER, Hex | 1 | MM74C906N | Nat'l Semiconductor |
| | *1mA maximum output current 2KΩ, 1/4W, 1% | | RN60C2001F | Mepco |
| | 5mA maximum output current 402Ω, 1/4W, 1% | | RN60C4020F | Mepco |
| | 20mA maximum output current 100Ω, 1/4W, 1% | | RN50C1000F | Mepco |
| | 50mA maximum output current 40.2Ω, 1/4W, 1% | | RN60C40R2F | Mepco |
| | **For channel update interval greater than 650 msec, 1 Meg Ω | | 4116R001-105 | |
| | For channel update interval less than 650 msec, 330K Ω | | 4116R001-334 | |
| | ***U4 and U34 not used on Models IAR-1 and IAR-2 | | | |

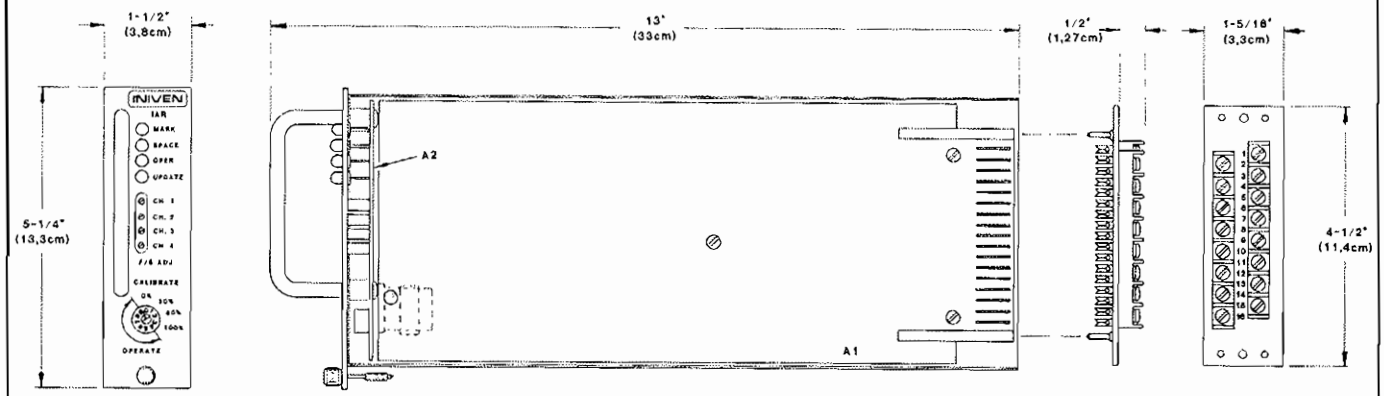



**Figure 5. IAR Analog Receiver—Dimensions and Component Identification**

| REF DESIG | DESCRIPTION | QTY | PART NUMBER | MFR |
|---|---|---|---|---|
| | IAR ANALOG RECEIVER ASSEMBLY | | | |
| | • HANDLE | | CC1181-XX | INIVEN |
| | • FACEPLATE | 1 | 230-18AL832C | Promptus Elec. |
| | • SCREW, Captive | 1 | 06B1181-OIN | INIVEN |
| | • CABLE ASSEMBLY | 1 | 08A1088-OIN | INIVEN |
| | • TERMINAL BLOCK ASSEMBLY | 1 | CA-D201DSS-E | Circuit Assy |
| A1 | • PRINTED CIRCUIT BOARD ASSY | 1 | CC1102-00 | INIVEN |
| | (See Figure 6 for breakdown) | 1 | AD1181-OIN | INIVEN |
| A2 | • PRINTED CIRCUIT BOARD ASSY | | | |
| | (See Figure 7 for breakdown) | 1 | AD1181-O2N | INIVEN |

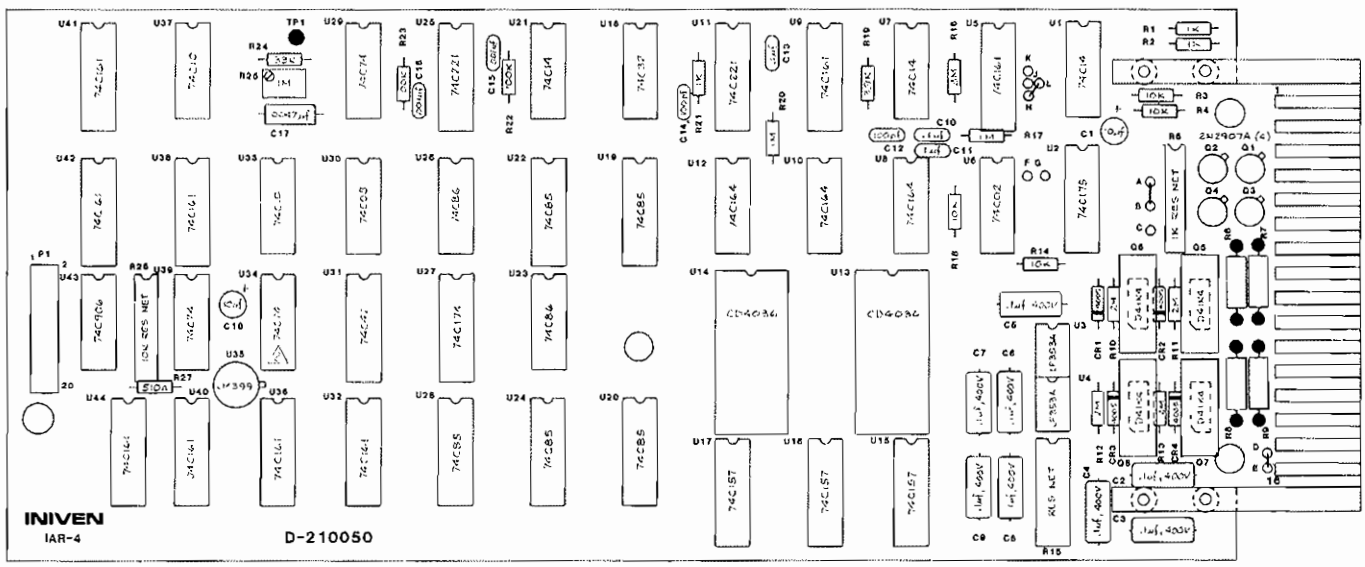



**Figure 6. Printed Circuit Board Assembly A1**

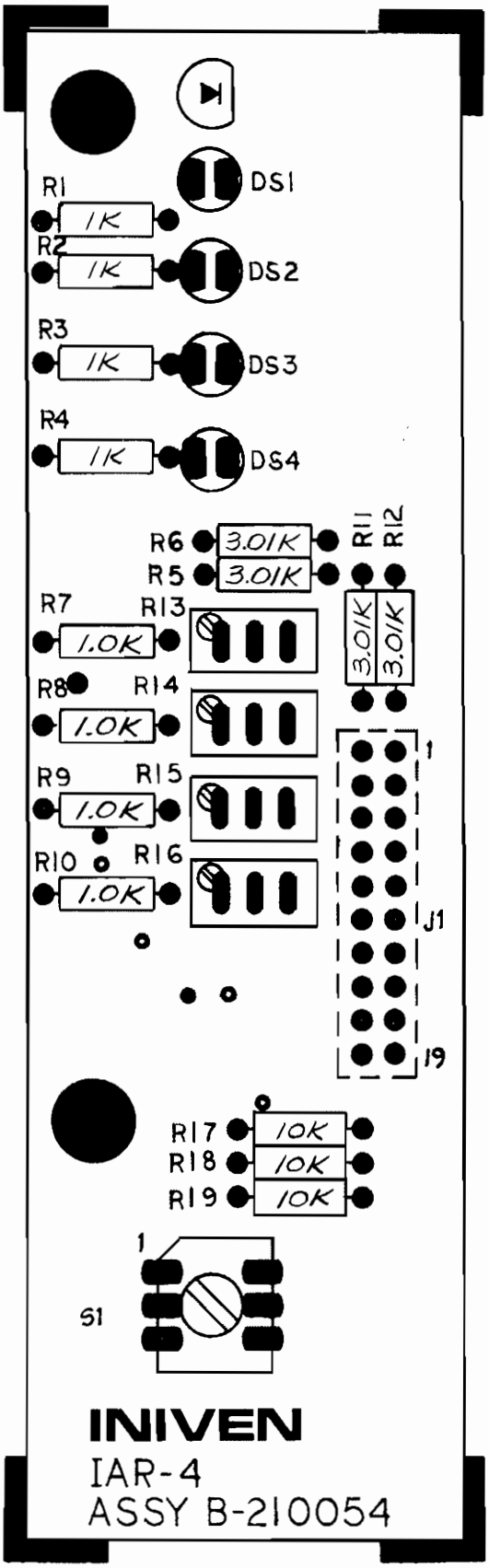



Figure 7. Printed Circuit Board Assembly A2

7.3 Printed Circuit Board Assembly A2. (See Figure 7)

| REF DESIG | DESCRIPTION |
|---|---|
| | PRINTED CIRCUIT BOARD ASSEMBLY A2 |
| DS1, DS4 | •LED, Red, 0.190 dia |
| DS2 | •LED, Yellow, 0.190 dia |
| DS3 | •LED, Green, 0.190 dia |
| J1 | •CONNECTOR, 20 Pin |
| R1-R4 | •RESISTOR, 1K, 1/4W, 5% |
| R5, R6, R11, R12 | •RESISTOR, 3.01K, 1/8W, 1% |
| R7-R10 | •RESISTOR, 1K, 1/8W, 1% |
| R13-R16 | •RESISTOR, Variable, 1K, 20 Turn |
| R17-R19 | •RESISTOR, 10K, 1/4W, 5% |
| S1 | •SWITCH, Rotary |

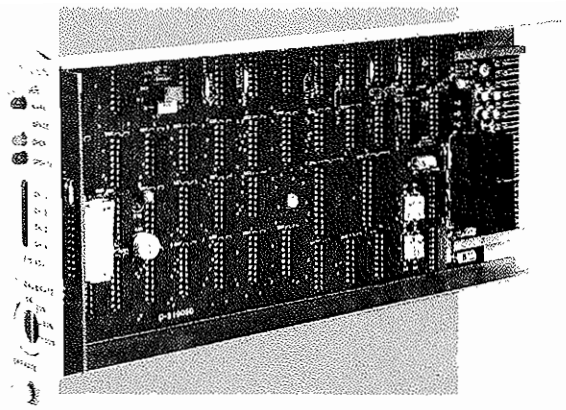
| QTY | PART NUMBER | MFR |
|---|---|---|
| 2 | 521-9212 | Dialco |
| 1 | 521-9176 | Dialco |
| 1 | 521-9175 | Dialco |
| 1 | CA-D20-SP100 | Circuit Assy |
| 4 | RCF07J102 | |
| 4 | RN55C3011F | |
| 4 | RN55C1001F | |
| 1 | 3299W-1-102 | Bourns |
| 3 | RCF07J103 | |
| 1 | 230002G | EECO |

## 8. ORDERING INFORMATION

8.1 When ordering please specify:

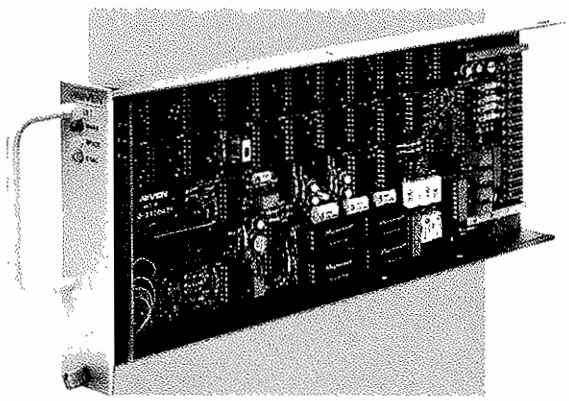
1. Model Number i.e. IAR-3 would specify a 3-channel analog receiver.
2. Baud Rate
3. Options: Output range. (Refer to section 2; Specifications)

8.2 When baud rate and/or output range are not specified, the IAR is set for 50 baud operation and 20mA maximum output current.



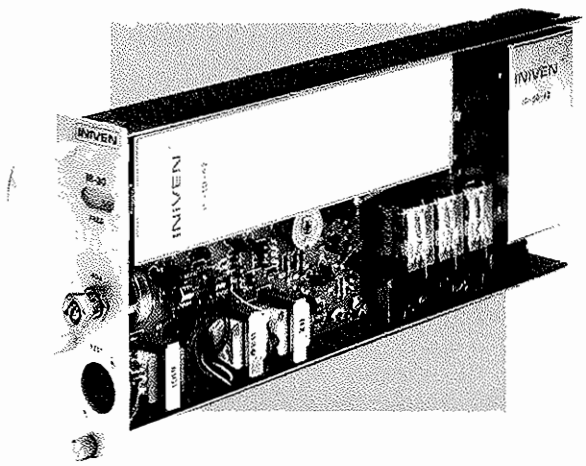
## IAR ANALOG RECEIVER

A state of the art digital-to-analog receiver which can provide up to 4 analog channels and 4 independent discrete outputs. The IAR decodes a 25 bit data word transmitted over an IT/IR-30 FSK channel for maximum security and accuracy.



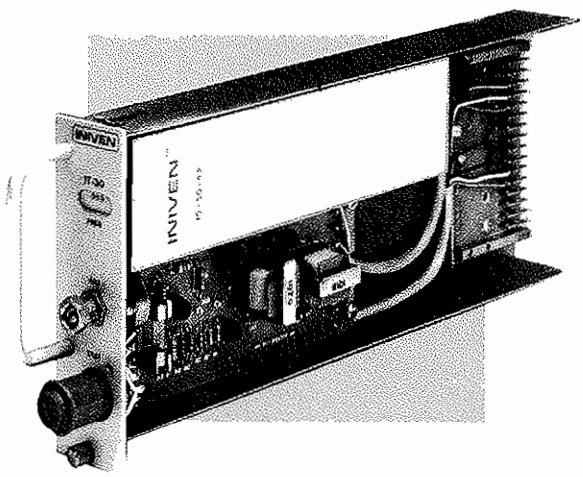
## IAT ANALOG TRANSMITTER

A high-performance solid-state analog-to-digital transmitter converts up to 4 analog and 4 independent discrete inputs for transmission over a single IT/IR-30 FSK channel.




## IR-30 FSK RECEIVER

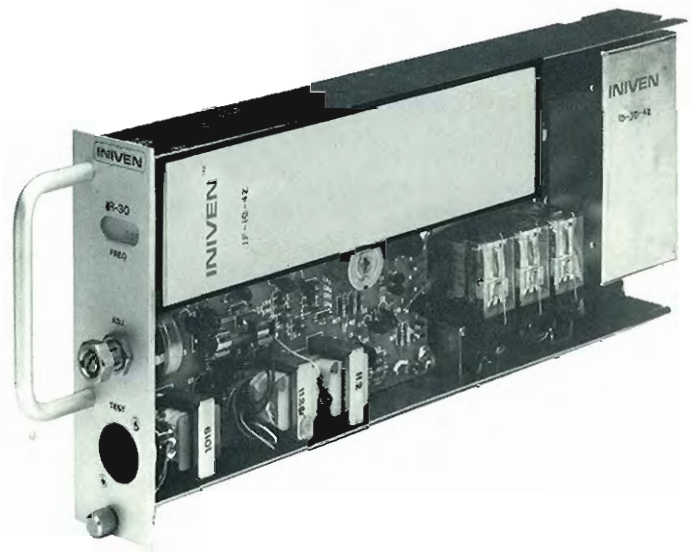
A frequency-shift-keyed (FSK) Tone Receiver for remote supervisory, telemetry, and data transmission applications. In response to a Mark, Space, or Center tone within its specified pass band, the IR-30 produces 3 separate contact closures (via relays) or voltage outputs (via adapters). Unique filtering provides maximum noise rejection for security in worst case conditions.



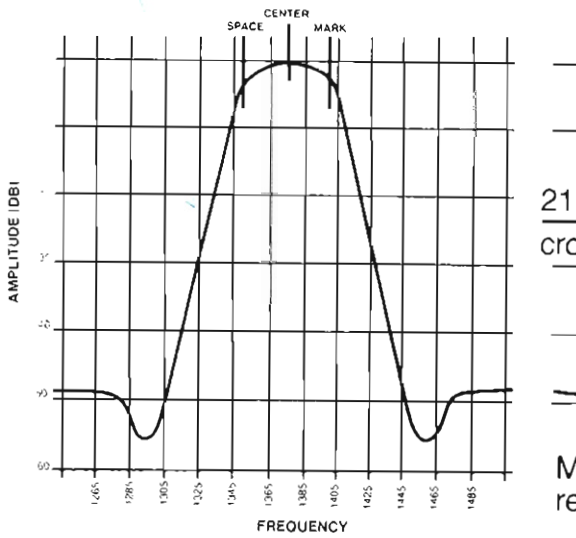

## IT-30

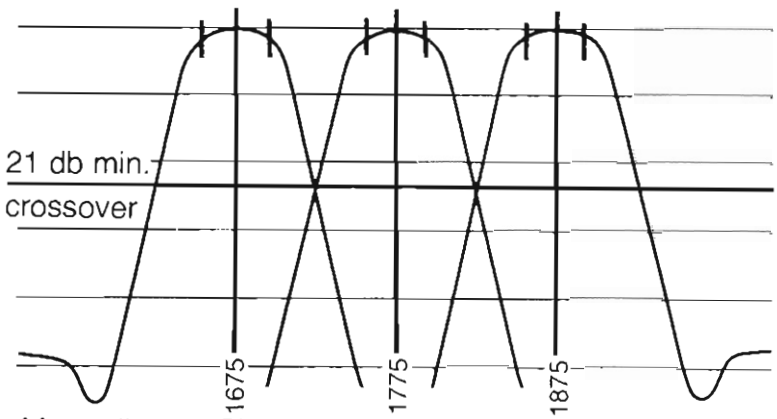
A frequency-shift-keyed (FSK) Tone Transmitter for remote supervisory, telemetry, and data transmission. The transmitter responds to contact or voltage keying to produce frequency shifts which are sent to an IR-30 FSK receiver. The IT/IR-30 form a highly reliable communication circuit.

# Only Iniven's unique filter designs reject adjacent channels by a minimum of 45DB. Providing maximum attenuation between adjacent channels.




**IF-10 FILTER***




Max adjacent Channel attenuation and max crossover rejection between channels (21 db. min.)

## FEATURES

Iniven's unique filter design is the product of years of engineering and development by Conolog, an acknowledged leader in communication system networks. The Iniven filter provides maximum noise rejection from out of band frequencies.

This standard feature eliminates receiver crosstalk even in the worst case conditions. Communication reliability with Iniven products provide the convenience of remote site supervision from your master station with unequaled consistent accuracy and security.

INIVEN™ A Subsidiary of Conolog Corporation

5 Columbia Rd. Somerville, N.J. 08876 (201) 722-3770

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