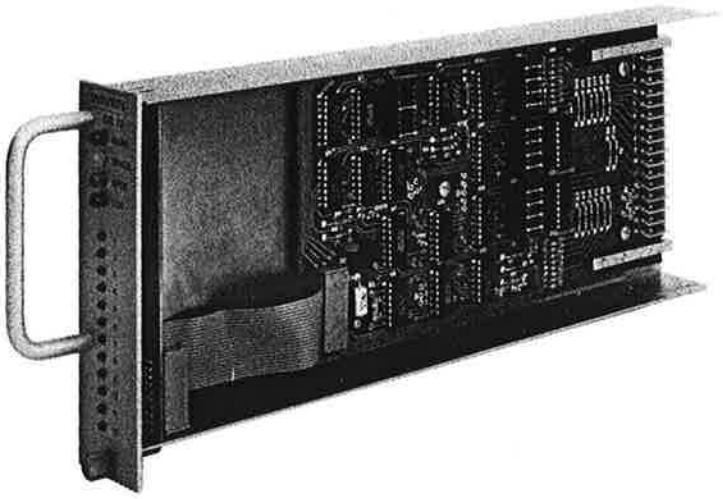
INIVEN™

Model ISR-12
SCANNER
RECEIVER

INSTRUCTION MANUAL



ISR-12 Scanner Receiver

1. DESCRIPTION

1.1 The INIVEN™ ISR-12 Scanner Receiver operates in conjunction with a standard IR-30 FSK Tone Receiver to receive serial tri-state RTZ data from a remote IST-12 Scanner/FSK Transmitter and convert the data to parallel outputs. The ISR-12 is housed in a standard INIVEN module with 15 LED-indicators mounted on the faceplate. Twelve LEDs are used to display last received status. Two LEDs display Mark and Space data received and one LED indicates the ISR-12 is receiving valid data. The transmission path is via a single 2-wire pair, such as a leased telephone line.

1.2 The ISR-12 receives a serial train of pulses via IA-11 voltage output adapters within the IR-30. The ISR-12 verifies this data for proper timing, pulse width, number of pulses, and sync pulse position. If the received data is in satisfactory format, it is gated to the outputs on the terminal block. Outputs can be used to activate lamps, relays, or other user connected loads.

1.3 Internal strap options permit the logic level of any point to be inverted. An optional, adjustable scan-fail output is provided.

2. SPECIFICATIONS

Reception Speed: 15, 20, 25, 30, and 40 data bits per second (approximately 60 percent of baud rate) are standard depending on channel spacing and bandwidth of tone receiver. 180 points per second maximum (300 baud).

Reception Mode: Serial asynchronous 12 bits plus 1 bit sync period. Three-state, return-to-zero code format. Optional 8-bit format.

Security: Pulse width, bit count, framing with RTZ sync period, and optional dual scan.

Input: Two-line (Mark/Space) connection to 12 Vdc bus for logic 1. (IR-30 Receiver with two IA-11 Adapters).

STATUS OUTPUTS

Number: 12 maximum. 11 when either scan-fail or Change of State (COS) are required externally; 10 when both scan-fail and COS are required externally. Power-on reset of all outputs until first valid scan(s) is received.

Power: Open-collector NPN transistor output capable of sinking up to 300 mA @ 100 Vdc maximum.

Logic Convention: Normal — Mark = Output ON
Inverted — Space = Output OFF

Operating Temperature: −30°C to +60°C (−22°F to +140°F)

Humidity: 0 to 95% non-condensing

Power Requirement: 12 Vdc ± 10%; 50 mA not including output load current

Weight: 2 lb approx. (0.9 Kg)

3. FEATURES

Normal/Inverted Output — The ISR-12 may be modified to reflect either ON or OFF output condition as the result of an active input.

Single Scan — The added security of double scan may be disabled.

Scan Fail Indication — Up to 15 scan fails may be allowed to occur prior to actuating the scan fail indicator circuit.

Memory — Status existing prior to a scan fail occurence may be retained, if desired.

COS Indication — The ISR-12 indicator flashes each time there is a change in data from the previous valid state.

OPER Indication — The ISR-12 may be modified to change the operate indicator to a data fail indicator.

External Indication — The ISR-12 may be modified to actuate an external COS or OPER indicator circuit.

4. THEORY OF OPERATION (See Figures 1 and 2)

4.1 The ISR-12 consists of the basic clock, FSK input interface, shift register, output buffer, power on reset circuit, output bits normal/invert strap field, display circuit, and control circuit.

4.2 Basic Clock. The basic clock circuit consists of Schmitt triggers U2-2 and U2-4 arranged in an oscillator configuration. The Schmitt triggers are adjusted to oscillate at a frequency of 80 to 320 Hz via potent iometer VR1 in the oscillator R-C network. The clock output from U2-4 (TP-3) is routed to the control circuit. The basic clock is set to run at 8× the baud rate.

4.3 FSK Input Interface. The FSK input interface consists of load resistors R5 and R7; Schmitt triggers U2-10 and U2-12; positive function NAND gates U8-4, U8-10, and U8-11; and R-C filter networks of R6/C2 and R4/C3. The positive transitions of Mark and Space signals applied via terminal block connections 3 and 4 are filtered by R-C networks R4/C3 and R6/C2 respectively. The filtered signals are inverted via Schmitt triggers U2-10 and U2-12 and routed to NAND gates U8-10 and U8-11 connected as latches with an output at TP2. When reception of a Mark signal causes the inputs at U8-13 and U8-5 to go LOW, the latch sets and its output at TP2 (DATA) goes HIGH. Conversely, reception of a Space signal causes LOW latch inputs at U8-6 and U8-8, and output TP2 goes LOW. During the RTZ transmission (center frequency) the latch output at U8-11 retains its previous state. The output at TP1 (MARK/SPACE) goes HIGH for reception of either Mark or Space signals and goes LOW during reception of center frequency. The MARK/SPACE signal is output to the timing signal generator and data bit counter in the control circuit. The DATA output is routed to the control circuit to the reset input of the timing signal generator to the COS latch and data comparator circuit and to the shift register.

4.4 CONTROL CIRCUIT.
The control circuit consists of a timing signal generator, data-bit counter, scan fail detector, COS latch and data comparator, and transfer control circuit.

4.5 Timing Signal Generator. Timing signal generator U7 is an 1-of-8 octal decoder with mutually exculsive outputs X^1 through X^7 and X^0 reflecting counts of 1 thorough 8 (count-1 through count-8), respectively. U7 accepts MARK/SPACE pulses, from the FSK input interface circuit, at its reset input (pin 15) and accepts clock inputs at pin 14. A HIGH signal (during the reception of MARK/SPACE pulses) causes U7 to reset and output X^0 goes HIGH. Absence of the reset signal (during reception of center frequency) allows U7 to advance to a count of 4 at clock rate. At count-1, the HIGH output at X^1 (DATA STROBE) is routed to the COS latch. At count-2, the HIGH output at X^2 (SHIFT) is routed to the shift register. (The outputs at X^3 thru X^5 are not connected externally.) During the sync interval, in addition X^1 and X^2 outputs, U7 advances to count-6 and the HIGH output at X^6 (SYNC) is routed to the COS latch and data comparator. If the sync interval exceeds count-6, the HIGH output at count-7 (SCAN FAIL RESET) is fed back to the enable input of U7 to prevent further counting until the next reset when a MARK/SPACE pulse is received. The SCAN FAIL RESET output is also routed to clear data bit counter U4.

4.6 Data Bit Counter. The data bit counter consists of one-half of dual 4-stage counter U4, dual 1-of-4 decoder U6 and associated circuitry. U4 and U6 are configured to decode a count of 12 MARK/SPACE pulses (a data word) accepted at U4-2 by outputting a LOW signal at U6-9. Any count other than 12 produces a HIGH output at U6-9 (COUNT-12) to the transfer control circuit.

4.7 Transfer Control Circuit. The transfer control circuit consists of XOR gate U11-11, NAND gate U15-4, and inverter U2-6. When a count other than 12 is sensed, a COUNT-12 signal from the data bit counter inhibits XOR gate U11-11 and deters generation of the TRANSFER signal via NAND gate 15-4 and inverter U2-6. When the COUNT-12 signal is LOW, gate U11-11 is enabled and a SYNC pulse applied at gate U15-15 is output at U2-6 as the TRANSFER signal. The TRANSFER signal is routed to reset the data-bit counter and is also routed to the scan fail detector and output buffer.

4.8 Scan Fail Detector. The scan fail detector consists of one-half of dual 4-stage counter U4, the entirety of dual 4-stage counter U1, 1-of-4 decoder U3, header U5 and associated circuitry. One-half of U4 and all of U1 are configured as an 11-stage counter with outputs at U1. The outputs of U1 are decoded via U3 and applied to header U5, where optional strapping permits selection of up to 15 scan fails to occur before the SCAN FAIL signal is fed back to disable the input to the 11-stage counter at U4 and output to the display circuit.

4.9 COS Latch and data Comparator. The COS latch and data comparator consists of XOR gates U11-3 and U11-10 and NAND gates U15-10, U15-3, and U8-3. U11-10 is the double scan comparator while U15-3 and 15-10 are configured as the latch with U11-3 and U8-3 as the set and reset inputs, respectively. The latch is held reset by +12 Vdc applied to U11-3 except in two instances: between each data-word at count-6 of the sync interval it is set by the SYNC signal from U7 and when a double scan comparison fails. At count-1 of center frequency transmission the Mark/Space input from the FSK input interface circuit is compared with its corresponding bit in the shift register from the previous scan at U11-10. If the bits match then the set input to the COS latch remains LOW and its output remains LOW. However; if the bit-comparison fails then the pin 2 input to the latch set input goes HIGH, resulting in a HIGH (COS) output from the latch. The COS output is routed to clear the data-bit counter and via inverter U21-12 to forward bias diode CR4 and light the COS indicator in the display circuit.

4.10 SHIFT REGISTER.
The shift register consists of dual 4-bit static shift register U10 and one-half of dual shift register U9 configured as a 12-stage shift register with parallel outputs to the output buffer. At each positive transition of the SHIFT signal accepted from U7, the DATA signal from the FSK interface is shifted to the next stage so that the data output at the 12th stage (U9-2) and the incoming data bit reflect the same scan point. When the transfer signal is sensed the data in the shift register is output via the output buffer.

4.11 OUTPUT BUFFER.
The output buffer consists of quad type D flip-flops U12, U13 and U14 having complementary outputs. The output buffer accepts parallel data transfers from the shift register and outputs either a normal (N) or inverted (I) output via the output bits normal/inverter strap field when the transfer signal is applied to its clock input. The output buffer also accepts the power-on reset signal at its reset input.

4.12 Power On Reset. The power on reset circuit consists of capacitor C1, resistor R1, diode CR1, and associated circuitry. The power-own reset circuit supplies a reset signal to the output buffer, via NAND gate U15-11 and Schmitt trigger U2-8 for a period as determined by the time constant of R1 and C1 whenever the 12-volt supply is turned on.

4.13 Display Circuit. The display circuit consists of LEDs DS1 through DS16. DS1 and DS2 are tied directly to the Mark and Space inputs from the tone receiver and illuminate to reflect reception of the respective signals. DS3 accepts signals from the scan fail circuit via inverter U21-10 and is normally illuminated when no scan fails occur. However, the display may be modified to remain off under no scan fail condition and illuminate when the selected number of scan fails is exceeded.

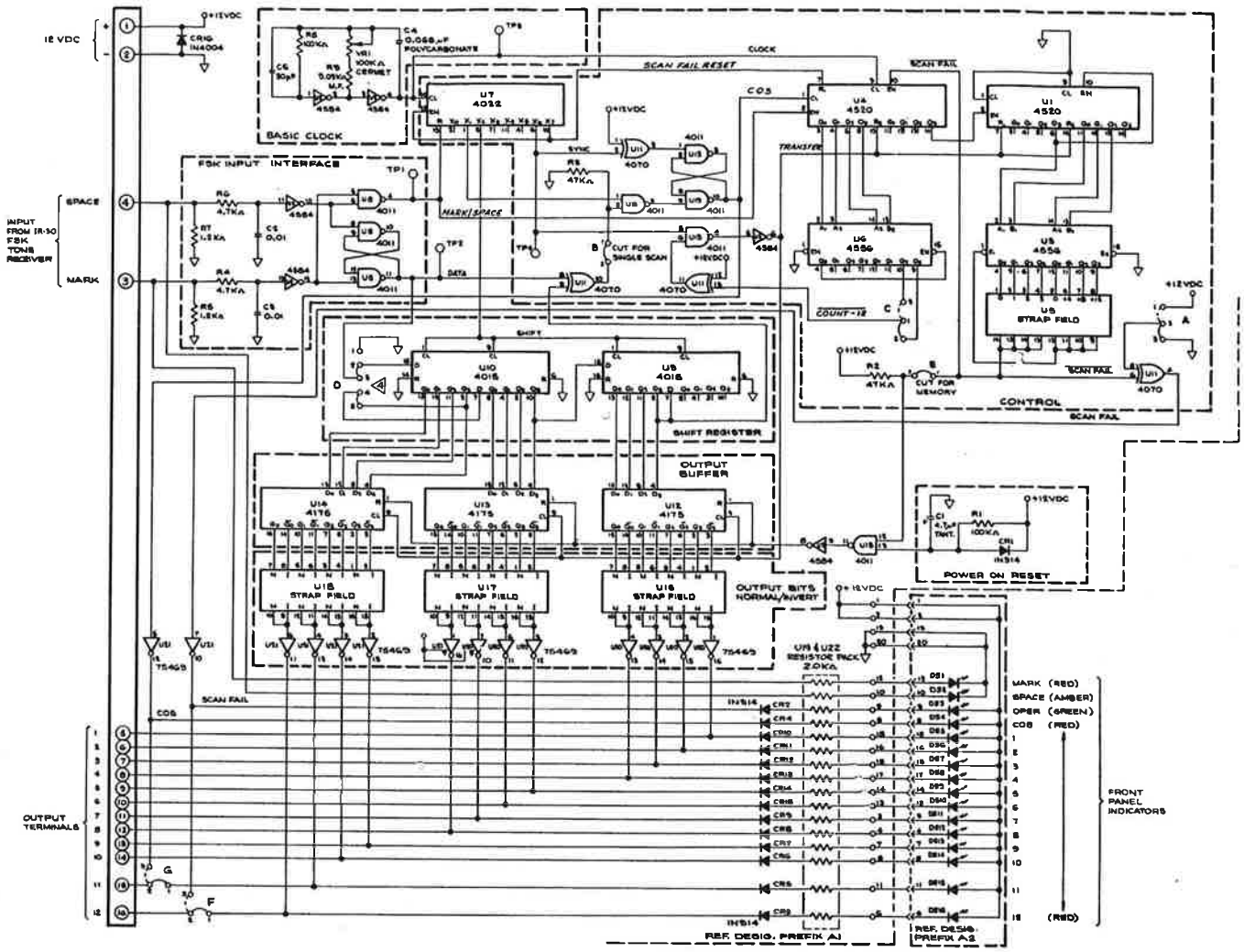


Figure 1. ISR-12 Scanner Receiver Schematic Diagram

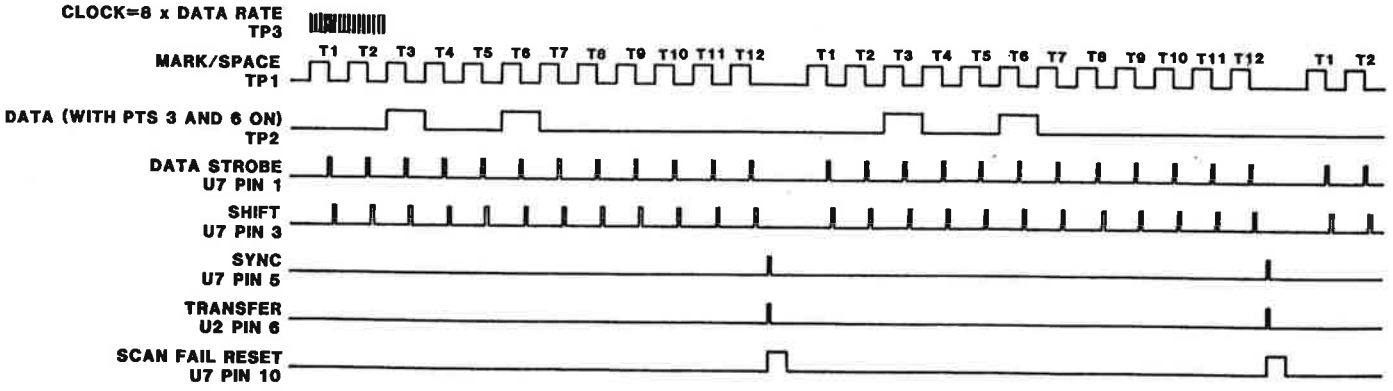


Figure 2. ISR-12 Timing Diagram

5. INSTALLATION

5.1 Unpacking. Unpacking and handling of the ISR-12 should be consistent with procedures used in handling electronic equipment.

5.2 Inspection. Visually inspect the ISR-12 for damage from rough handling and faulty packing. Visually inspect for:

(1) Loose Wires

(2) Deformation in the frame

(3) Faceplate damage

(4) Evidence of moisture or condensation within the units.

(5) Loose hardware or parts which evidence improper handling.

5.3 Mechanical Installation. The ISR-12 is shipped with the terminal block plugged in and secured to the rear of the unit by four 6-32 screws. The ISR-12 is normally mounted in standard INIVEN™ Tone Frames.

5.4 Install the ISR-12 as follows:

(1) Leave terminal block plugged in, as shipped, on rear of unit.

(2) Remove four 6-32 screws from terminal block.

(3) While inserting ISR-12 into tone frame align captive screw at bottom of faceplate with mounting hole in frame.

(4) Secure ISR-12 to frame using captive screw on faceplate.

(5) At rear of frame, use 6-32 screws removed in step (2) to secure terminal block to tone frame.

The ISR-12 can now be removed and re-installed in the frame using the front panel captive screw.

5.5 Electrical Installation. All electrical connections are made to the terminal block at the rear of the frame (see figure 3 and Table 5-1).

Table 5-1. Terminal Block Connections

TERMINAL	FUNCTION
1	Positive (+) side of 12 Vdc power supply input.
2	Negative (−) side of 12 Vdc power supply input.
3	Mark input.
4	Space input
5 through 16	Outputs for points 1 through 12

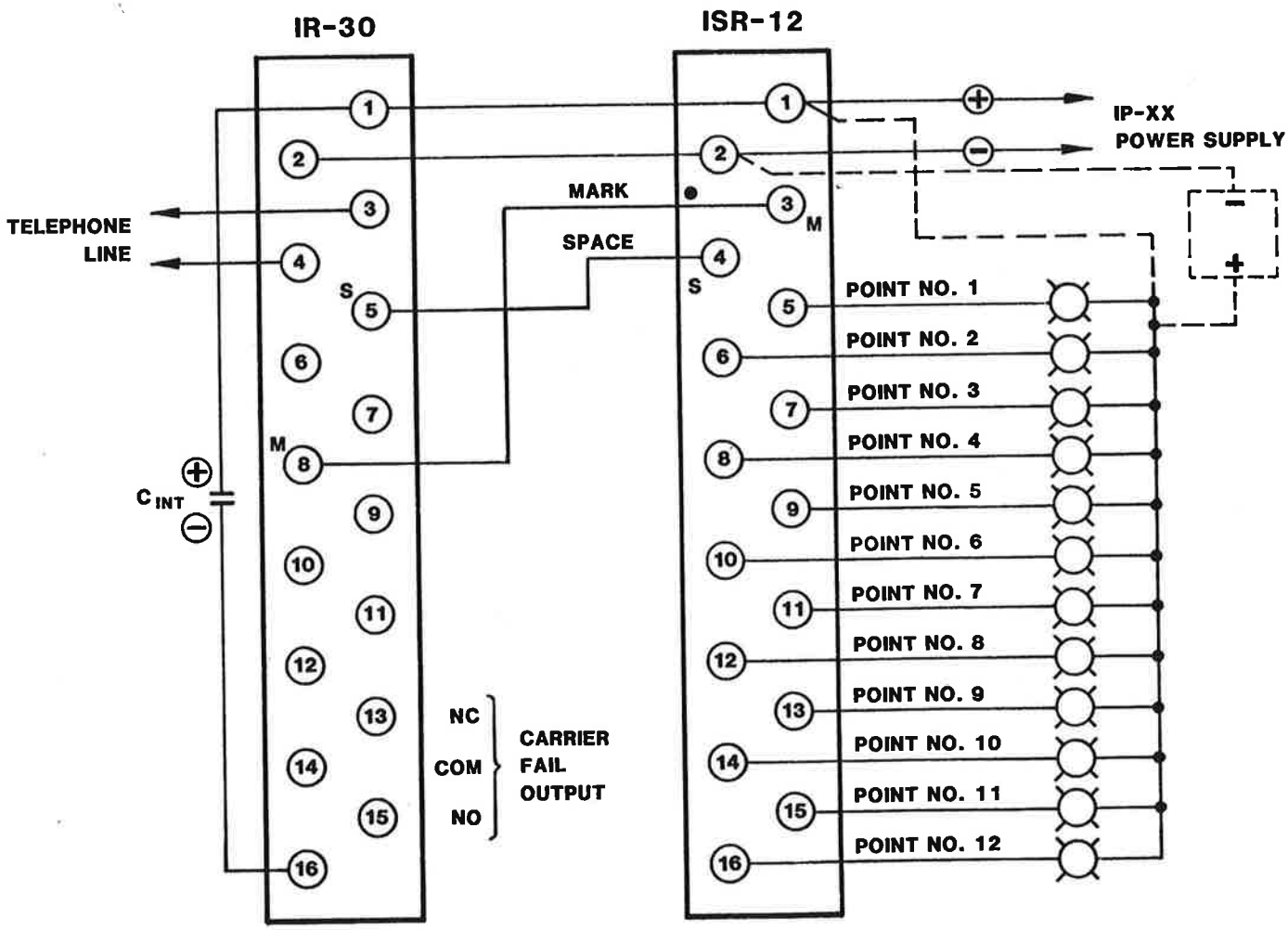


Figure 3. Electrical Installation

5.6 Electrical Grounding. It is recommended that the chassis of each tone unit is grounded to reduce group loop interference effects. When the tone unit is housed in a standard INIVEN™ Tone frame, a good earth-ground to the rack or other equipment in which the frame is installed, is sufficient. When the individual tone units are operated out of the frame, each tone unit chassis should be connected to earth-ground.

5.7 Clock Adjustment
The following equipment is required to set the clock rate of the ISR-12 Scanner Receiver:

Freq. Counter	**Fluke**	**Model 1900A (or equiv.)**
Extender Module	**INIVEN**	**IE-5**

NOTE

The clock output should be adjusted to a frequency which is eight times (8X) the baud rate.

5.8 Adjustment Procedure

(1) Loosen captive retaining screw and remove ISR-12 from frame.

(2) Plug ISR-12 into Extender Module.

(3) Install Extender Module in space vacated by ISR-12.

(4) Ground Frequency Counter to terminal 2 of connector and connect test probe to test point TP3 on printed circuit board A1 (See figure 5).

(5) Frequency Counter should indicate a frequency eight times (8X) the baud rate: if not, proceed to step (6). (For example 400Hz = 50 baud.)

(6) Rotate adjustment screw on potentiometer A1VR1 to obtain desired indication on the Frequency Counter.

(7) Disconnect Frequency Counter from test point and terminal 2.

(8) Remove Extender Module from frame and unplug ISR-12 from Extender Module.

(9) Install ISR-12 in frame and secure with captive retaining screw.

5.9 OPTIONAL OPERATION ADJUSTMENTS.

Various optional adjustments of the ISR-12 are available to the user and can be accomplished prior to placing the unit in operation.

5.10 Scan Fail Option. Up to 15 scan fails may be allowed to occur before the OPER indicator reflects this condition. The units are set at the factory to allow 15 scan fail occurrences. To select the number of scan fails permitted; install jumpers on header U5 of printed circuit board A1 (figure 5) in accordance with table 5-1.

Table 5-1 Scan Fail Options

SCANS	JUMPER	SCANS	JUMPER
0	1 to 16 5 to 12	8	1 to 16 10 to 7
1	2 to 15 5 to 12	9	2 to 15 10 to 7
2	3 to 14 5 to 12	10	3 to 14 10 to 7
3	4 to 13 5 to 12	11	4 to 13 10 to 7
4	1 to 16 6 to 11	12	1 to 16 9 to 8
5	2 to 15 6 to 11	13	2 to 15 9 to 8
6	3 to 14 6 to 11	14	3 to 14 9 to 8
7	4 to 13 6 to 11	15	4 to 13 9 to 8

5.11 Eight Point Scan Option. To modify the ISR-12 to monitor eight points, proceed as follows:

NOTE

A similar adjustment must be made on the matching ISR-12 Scanner/FSK Transmitter for the system to perform satisfactorily.

(1) Cut the following etches on printed circuit board A1 (figure 5).

C1 to C2 D2 to D3 D4 to D5

(2) Add the following jumpers on printed circuit board A1.

C1 to C3 D1 to D2 D3 to D4

5.12 OPER Indication Option. The unit is wired at the factory so that the OPER indicator remains ON as long as the number of successive scan fails does not exceed the permitted quantity. The OPER indication may be reversed to remain off as long as the allowed number of successive scan fails is not exceeded. To reverse the OPER indicator status significance, cut etch on printed circuit board A1 (figure 5) between A2 and A3 and install a jumper from A1 to A2.

5.13 Normal/Inverted Output Option. Units are shipped from the factory wired to reflect the logic convention: input contact closed=Mark=Output ON. If it is desired to use the convention: Input contact closed=Mark=Output OFF remove headers U16 through U18, (figure 5) from sockets and reinstall in reverse configuration (i.e. pin 1 to pin 16). Inverted outputs may be selected for discrete points by removing the associated jumper between the header pins labeled N on figure 2 and reinstalling the jumper between the header pins labeled 1.

5.14 Scan Fail Memory Option. The ISR-12 is configured so that status in the output buffer is not retained subsequent to a scan fail occurrence. It if is desired to retain status conditions existing prior to the scan fail, cut the etch on printed circuit board A1 (figure 5) at point E.

5.15 Single Scan Option. If the added security of double scan is not desired, cut the etch on printed circuit board A1 (figure 5) at point B.

5.16 External OPER Indication Option. If it is desired to use an external circuit for indication of OPER status significance, scan point 12 must be eliminated. To use an external circuit for OPER status proceed as follows:

(1) Cut etch on printed circuit board A1 (figure 6) between G1 and G2.

(2) Install a jumper from G2 to G3.

(3) Connect external COS indicator circuit to terminal 16 of terminal block.

NOTE

Relay will remain energized during normal operation.

5.17 External COS Indication Option. If it is desired to use an external circuit for indication of change-of-state, scan point 11 must be eliminated. To use an external circuit for indication of change-of-state, proceed as follows:

NOTE

The COS output is a pulse with a variable of from 1 to 12 data bit periods (MARK/SPACE, figure 2). An external latch circuit should be used if memory of COS is desired.

(1) Cut etch on printed circuit board A1 (figure 5) between F1 and F2.

(2) Install a jumper from F2 to F3

(3) Connect external COS indicator circuit to terminal 15 of terminal block.

5.18 If it is desired to have only external COS indication without external OPER indication, scan point 12 may be used instead of scan point 11. Proceed as follows:

(1) Cut etch on printed circuit board A1 (figure 6) between G1 and G2.

(2) Install a jumper from F3 to G2.

(3) Connect external COS indicator circuit to terminal 16 of terminal block.

6. MAINTENANCE

This section contains corrective maintenance procedures that can be used in conjunction with the adjustment procedures in Section 5.

6.1 The module you have purchased has been thoroughly inspected and tested in accordance with our specifications. The module does not require preventive maintenance. However, it is recommended that clock signals be checked and adjusted every 6 months.

6.2 In-plant quality assurance procedures specify transmission levels that vary for "hardware" and "system" orders. Testing the modules, in either case, is over a transmission link simulating a telephone circuit (600 ohms impedance) with a loss of 25 dbm from origin to destination. The attenuation and frequency response of the circuit is due to a number of factors which cannot be duplicated at the factory. The factors include:

(1) Distance between stations.

(2) Diameter and length of wire used in transmission circuit.

(3) Actual impedance of transmission circuit.

(4) Inductance and capacitance of transmission circuit.

6.3 Quick-Check — Table 6-1 contains quick-check procedures designed to isolate trouble in the majority of cases. When use of these procedures fails to locate the cause of the malfunction, refer to Section 4 for detailed theory of operation and the referenced schematics as an aid in signal tracing.

Table 6-1. Quick Check Malfunction Isolation

SYMPTOM	POSSIBLE CAUSE	REMEDY
	SYSTEM CHECKS	
No operation.	Power failure of commercial power or IP power supply.	Check voltage.
	Transmission circuit failure.	Call telephone company for responsible agency.
Intermittent operation of some tone receivers.	Signal level shifted due to transmission circuit change.	Check all tone receivers to see if sensitivity has been affected. If so, notify responsible agency of change in circuit attenuation. Refer to Table 8-1 and adjust levels as necessary.
Tone receivers in "off" condition exhibit erratic and unsteady symptoms when checked using multimeter and Test Adapter.	Transmitter outputs set too high.	Check with telephone company or responsible agency for correct settings. Refer to Table 8-1, and adjust levels as necessary.
	Telephone company circuit trouble.	Call telephone company and advise of problem.
	Grounded telephone company circuit or defective filter or oscillator.	Determine if ground is on telephone line or due to tone equipment by measuring each side of line to ground with line connected and then disconnected from equipment. If ground is due to tone equipment, it may be caused by a defective oscillator or filter. Pull out each module in turn while monitoring ground with multimeter until absence of low resistance indication signifies module containing defective filter or oscillator.

7. PARTS LIST

7.1 The following parts list is included to facilitate maintenance of the ISR-12. All parts are listed in the order of their reference designators, as applicable. Figure 4 depicts the parts for the major components and assemblies. Figures 5 and 6 exhibits parts for printed circuit board A1 and printed circuit board A2, respectively.

7.2

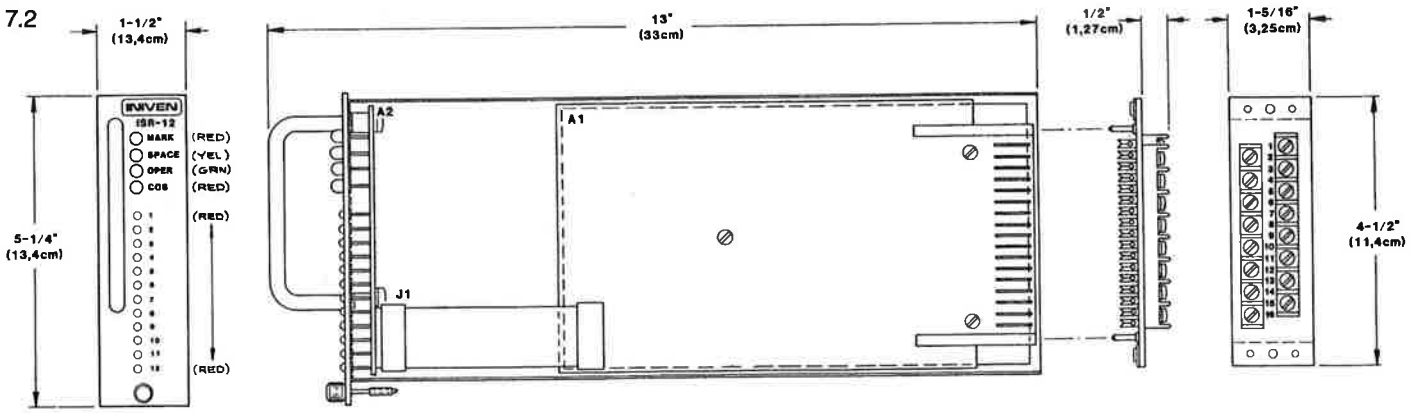


Figure 4. ISR-12 Scanner Receiver — Dimensions and Component Identification

REF DESIG	DESCRIPTION	QTY	PART NUMBER	MFR
	ISR-12 SCANNER RECEIVER ASSEMBLY		CC1177-00	INIVEN
	• HANDLE	1	23018AL832C	Promptus Elec.
	• FACEPLATE	1	06B1177-OIA	INIVEN
	• SCREW, Captive	1	08A1088-OIN	INIVEN
	• TERMINAL BLOCK ASSEMBLY	1	CC1102-00	INIVEN
A1	• PRINTED CIRCUIT BOARD ASSY (See figure 6 for breakdown)	1	AD1177-OIN	INIVEN
A2	• PRINTED CIRCUIT BOARD ASSY (See figure 7 for breakdown)	1	AD1177-02N	INIVEN

REF DESIG	DESCRIPTION	QTY	PART NUMBER	MFR
	PRINTED CIRCUIT BOARD ASSEMBLY A1		AD-1177OIN	INIVEN
C1	• CAPACITOR, 4.7uf, 35V	1	DT35V475M	
C2, C3	• CAPACITOR, 0.01uf, 25V, cer	2	CGY5P103M	
C4	• CAPACITOR, 0.068uf, 50V, Polycarb	1	MPC32D683J	
C5	• CAPACITOR, 100pf, 1KV, 10%		CGX5F101K	
CR1-CR15	• DIODE	15	1N914	Fairchild
CR16	• DIODE, Silicon, 1 Amp, 400V	1	1N4004	Motorola
	• CABLE ASSEMBLY	1	60001	BELDON
R1	• RESISTOR, 100K, 1/4 W, 5%	1	RCF07J104	
R2, R3	• RESISTOR, 47K, 1/4 W, 5%	2	RCF07J473	
R4, R6	• RESISTOR, 4.7K, 1/4 W, 5%	2	RCF07J472	
R5, R7	• RESISTOR, 1.2K, 1/4 W, 5%	2	RCF07J122	
R8	• RESISTOR, 100K, 1/4 W, 1%	1	RN55F1003F	
R9	• RESISTOR, 9.09K, 1/8 W, 1%	1	RN55F9091F	
U1, U4	• COUNTER, Dual Binary Up	2	MC14520BCP	Motorola
U2	• SCHMITT TRIGGER, Hex	1	MC14584BCP	Motorola
U3, U6	• DECODER/DEMUX, Dual 1-of-4	2	MC14556BCP	Motorola
U7	• COUNTER/DIVIDER, Octal	1	MC14022BCP	Motorola
U8, U15	• NAND GATE, Quad 2-input	2	MC14011BCP	Motorola
U9, U10	• SHIFT REGISTER, Dual 4-Bit Static	2	MC14015BCP	Motorola
U12-U14	• FLIP-FLOP, Quad Type D	3	MC14175BCP	Motorola
U20, U21	• INTERFACE, Darlington Transistor Array	2	SN75469N	Texas Instrument
	• ADAPTOR PLUG ASSY	4	702-35050104	Cambion
	• DIP SOCKET, Low Profile, 14 Pin	4	703-53140104	Cambion
	• DIP SOCKET, Low Profile, 16 Pin	18	703-53160104	Cambion
VR1	• RESISTOR, Variable, 100K	1	64Y104	Spectrol
U19, U22	• RESISTOR PACK, 16 Pin DIP 2K, 1/4 W, 2%	2	4116R001-202	Bourns

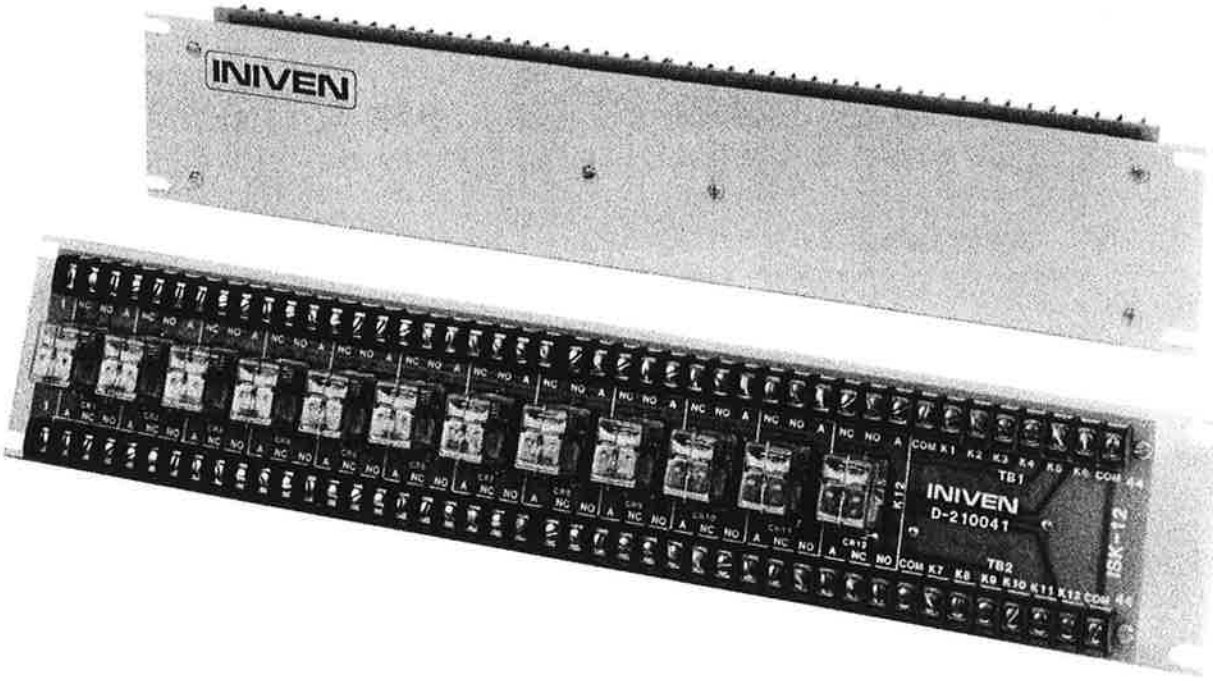


Figure 7. ISK-12 Relay Panel

9. ISK-12 RELAY PANEL (See figures 7 and 8)

9.1 The ISK-12 relay panel is a 19-inch wide by 3-15/32-inch high by 3-in deep (with relays installed) standard RETMA rack-mountable panel.

The panel is available with up to 12 DPDT, plug-in relays. Each relay provides 2 Form C outputs with single-point contacts rated at 5 A @ 29 Vdc or 115 Vac (non-Inductive). The 230-ohm, 12-volt coil is driven by the ISR-12 outputs. A diode mounted across each coil provides transient suppression at the source to protect the solid-state outputs.

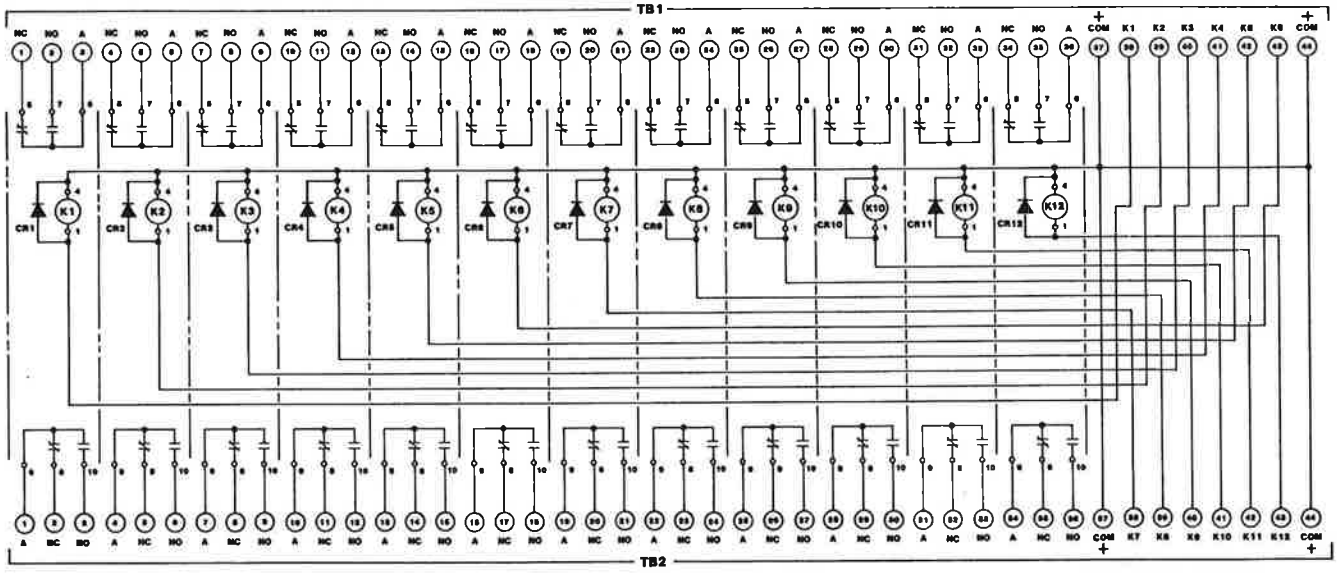


Figure 8. ISK-12 Relay Panel Schematic Diagram